What is claimed is:

1. A low power a reconfigurable processor core, comprising:

one or more processing units, each unit having a clock input that controls the performance of the unit;

one or more clock controllers having clock outputs coupled to the clock inputs of the processing units, the controller operating varying the clock frequency of each processing unit to optimize speed and processing power for a task; and

a high-density memory array core coupled to the processing units.

2. The processor core of claim 1, wherein the reconfigurable processor core includes one or more digital signal processors (DSPs).

3. The processor core of claim 1, wherein the reconfigurable processor core includes one or more reduced instruction set computer (RISC) processors.

4. The processor core of claim 1, wherein the processing unit includes:

a central processing unit (CPU) having a clock input coupled to the controller; and

a buffer adapted to be read by the CPU, the buffer having a clock input coupled to the controller.

5. The processor core of claim 1, wherein the CPU and the buffer are commonly clocked.

6. The processor core of claim 1, wherein the CPU and the buffer are separately clocked.

7. The processor core of claim 4, further comprising a second buffer adapted to receive data from the CPU, the buffer having a clock input coupled to the controller.

8. The processor core of claim 7, wherein the CPU, first and second buffers are commonly clocked.

9. The processor core of claim 7, wherein the CPU, first and second buffers are separately clocked.

10. The processor core of claim 4, wherein each CPU further comprises:

a private instruction random access memory coupled to the CPU; and

a private data random access memory coupled to the CPU.

11. A method for clocking one or more processing elements, each element including a central processing unit (CPU) having a processor clock input, a first buffer adapted to be read by the CPU and a second buffer adapted to receive data from the CPU, each buffer having a clock input, the method comprising:

varying the clock input to the processor and the first buffer based on the fill status of the first buffer; and

varying the clock input to the processor and the second buffer based on the fill status of the second buffer.

12. The method of claim 11, wherein the varying the clock input to the processor and the second buffer based on the fill status of the second buffer further

comprises slowing down or stopping the clock if the second buffer is above its high water mark or if the second buffer is full.

13. The method of claim 11, wherein the varying the clock input to the processor and the first buffer based on the fill status of the first buffer further comprises slowing down or stopping the clock if the first buffer is below its low water mark or if the first buffer is empty.

14. The method of claim 11, wherein the varying the clock input to the processor and the second buffer based on the fill status of the second buffer further comprises increasing the clock if the second buffer is below its low water mark or if the second buffer is empty.

15. The method of claim 11, wherein the varying the clock input to the processor and the first buffer based on the fill status of the first buffer further comprises increasing the clock if the first buffer is above its low water mark or above its empty level.

16. The method of claim 11, wherein the processor, the first buffer and the second buffer uses a common clock.

17. The method of claim 11, further comprising:

slowing down or stopping the clock if the second buffer is above its high water mark or if the second buffer is full;

slowing down or stopping the clock if the first buffer is below its low water mark or if the first buffer is empty;

increasing the clock if the second buffer is below its low water mark or if the second buffer is empty; or

increasing the clock if the first buffer is above its low water mark or above its empty level.

18. A low power a reconfigurable processor core, comprising:

one or more processing units, each unit having a clock input that controls the performance of the unit, each unit coupled to a source buffer and a destination buffer; and

means for varying the clock input to the processing unit, the first buffer and the second buffer based on the fill status of the buffers and high and low water marks.

19. The processor core of claim 18, wherein the water mark is fixed or programmable.

20. The processor core of claim 18, wherein the processing unit and the buffers are commonly clocked.